

What is Claimed is:

1 1. In a processing system having an unprotected
2 pipeline, an apparatus comprising:

3 a first logic gate for providing a first signal when a
4 halt signal and a non-interruptible code signal occur
5 together, and

6 a memory unit for storing the first signal, the first
7 signal indicating a non-returnable interruption of the
8 executing procedure.

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10 2. The apparatus as recited in claim 1 wherein the
11 first signal is transferred to a read bus.

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13 3. The apparatus as recited in claim 1 wherein the
14 memory unit is a memory-mapped register location.

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16 4. The apparatus as recited in claim 1 wherein the
17 first logic gate is a logic AND gate.

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19 5. The apparatus as recited in claim 1 further
20 comprising:

21 a second logic, and

22 a memory unit, the second logic gate providing a halt
23 signal when a trigger signal is applied to a first input
24 terminal and the contents of the memory unit are applied to
25 a second input terminal.

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2 6. A method for transferring a halt signal when a
3 halt signal occurs during a non-interruptible portion of
4 the executing code of a processor having a non-protected
5 pipeline, the method comprising:

6 determining when a halt signal occurs during a non-
7 interruptible portion of the executing code, and

8 storing a non-returnable bit in a memory location
9 accessible to testing device.

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11 7. The method as recited in claim 6 wherein, when
12 the control signal is applied to the memory location,
13 applying the non-returnable bit to a read bus.

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15 8. The method as recited in claim 7 wherein the
16 memory unit is a memory-mapped register.

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18 9. A data processing unit comprising:

19 a processor, the processor including:

20 a non-protected pipeline,

21 the processor executing interruptible code and
22 non-interruptible code;

23 an event signal generating unit, the event signal
24 generating unit generating an event signal in response to a
25 halt condition;

1 a logic unit responsive to the halt condition and
2 a control signal for generating a halt trigger signal
3 during a non-interruptible code portion; and
4 a storage unit for storing a non-returnable bit
5 in response to the trigger halt signal.

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7 10. The processing unit as recited in claim 9 wherein
8 the storage unit is a memory-mapped register, the memory
9 mapped register responsive to a control signal for
10 transferring the non-returnable bit outside of the
11 processor.

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13 11. The processing unit as recited in claim 10
14 further including a storage unit, the storage unit storing
15 an first signal when the processing unit is executing non-
16 interruptible code, the first signal stored in the storage
17 unit providing the control signal.